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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,938	06/23/2000	Michael T. Moore	CY-0011	1019

7590 03/10/2004

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/602,938	MOORE, MICHAEL T.	
	Examin r	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *05 January 2004* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicants' amendment of *1/05/04*.

1.1 Claims **1-20** remain pending.

1.2 The prior art rejections of record are withdrawn in response to Applicants' amendment of *1/05/04*.

1.3 The objections of record to the drawings are withdrawn in response to Applicants' amendment of *1/05/04*.

Response to Arguments

2. Applicants' arguments of ***1/05/04*** are persuasive only to the extent that self-testing is not described in detail prior art of record. However, **Abramovici et al.** (US Patent No. 6,631,487; filed: Sep. 27, 1999) discloses such self-testing, e.g., in Figs. 2-3 and col. 2 line 1 et seq.

Claim Rejections - 35 USC ' 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3.0 The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3.1 **Claims 1-20** are rejected under 35 U.S.C. 102 (e) as being anticipated by **Abramovici et al.** (US Patent No. 6,631,487; filed: Sep. 27, 1999).

Abramovici et al. anticipates the claimed invention because, e.g., in Figs. 2-3 and col. 2 line 1 et seq., *"An FPGA includes a plurality of programmable logic blocks and a plurality of*

programmable routing resources interconnecting the programmable logic blocks initially configured as an initial self-testing area for testing at least a portion of the programmable routing resources and/or programmable logic blocks for faults, and an initial working area for maintaining normal operation of the FPGA during testing. The portion of the programmable routing resources and/or programmable logic blocks located within the initial self-testing area are further subdivided and tested until the faulty programmable routing resource or programmable logic block is identified.

Fig. 2

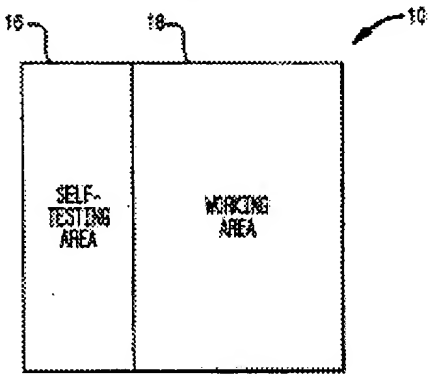


FIG. 2 is an illustration of an FPGA under test configured into an initial self-testing area and a working area wherein the working area maintains normal operation of the FPGA under test; FIG. 3 is an illustration of the FPGA under test configured such that the working area is divided into four disjoint areas by a vertical self-testing area and a horizontal self-testing area; FIG. 4 is a schematic block diagram showing a preferred comparison-based self-testing area configured to include a test pattern generator, an output response analyzer, and two groups of FPGA resources under test;.."

As per Claims 1-20, Abramovici et al. depicts, in **Figs. 1-9** and related description in ***col. 2 line 1 et seq.***, the claimed PLD or FPGA assembly comprising: programmable logic circuit

or array and nonvolatile memory or store for self-testing or BIST with means to store configuration data in plural modes such as operation or test or self-test modes. JTAG access port is provided for test and data communication and means to integrate all PLD or FPGA assembly within on die or IC. Means to reconfiguration circuit elements, such in circuit elements seen e.g., in Figs. 1-9 as ROM or EEPROM mask read-only memory in a manner clear to those skilled in the art how to partition memory in plural sectors for storing data or self-test data. Means to start or boot up said assembly via commands or microprocessor control means in cols. 1-14.

Figs. 1-9 show means for testing and self-testing similar to the claimed invention.

3.2 To anticipate under section 102, a prior art reference must disclose all the elements of the claimed invention or their equivalents functioning in essentially the same way. The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in ***Kalman v. Kimberly-Clark Corp.*** 713 F.2d 760, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984) it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations in the claim are found in the reference, or 'fully met' by it." The Examiner respectfully submits that all the limitations of Claims 1-20, or their equivalents functioning in essentially the same way, are found in the **Abramovici et al.** reference.

3.3 Examiner also notes that claims 1-20 read on Applicant's admitted prior Figs. 8a-c since Figs. 8a-c disclose the limitations of claims 1-20, and that Figs. 2a-c are merely relocating simple elements of the admitted prior Figs. 8a-c. It has been held that mere relocation of parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.1 **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sharma et al.** (US Patent No. 5,878,051; March 2, 1999). in view of **Abramovici et al.** (US Patent No. 6,631,487; filed: Sep. 27, 1999).

As per Claims 1-20, Sharma et al. renders obvious the claimed invention because, e.g., col. 3 line 23 et seq., as depicted in Figs. 1-3, describes: "*After the step of operating the assemblage and the field-programmable gate array as tester for testing the first type of logical function, the field-programmable gate array is reconfigured to either perform the particular function in the normal operating mode, or to perform a test on a second type of logical function in a further self-test*

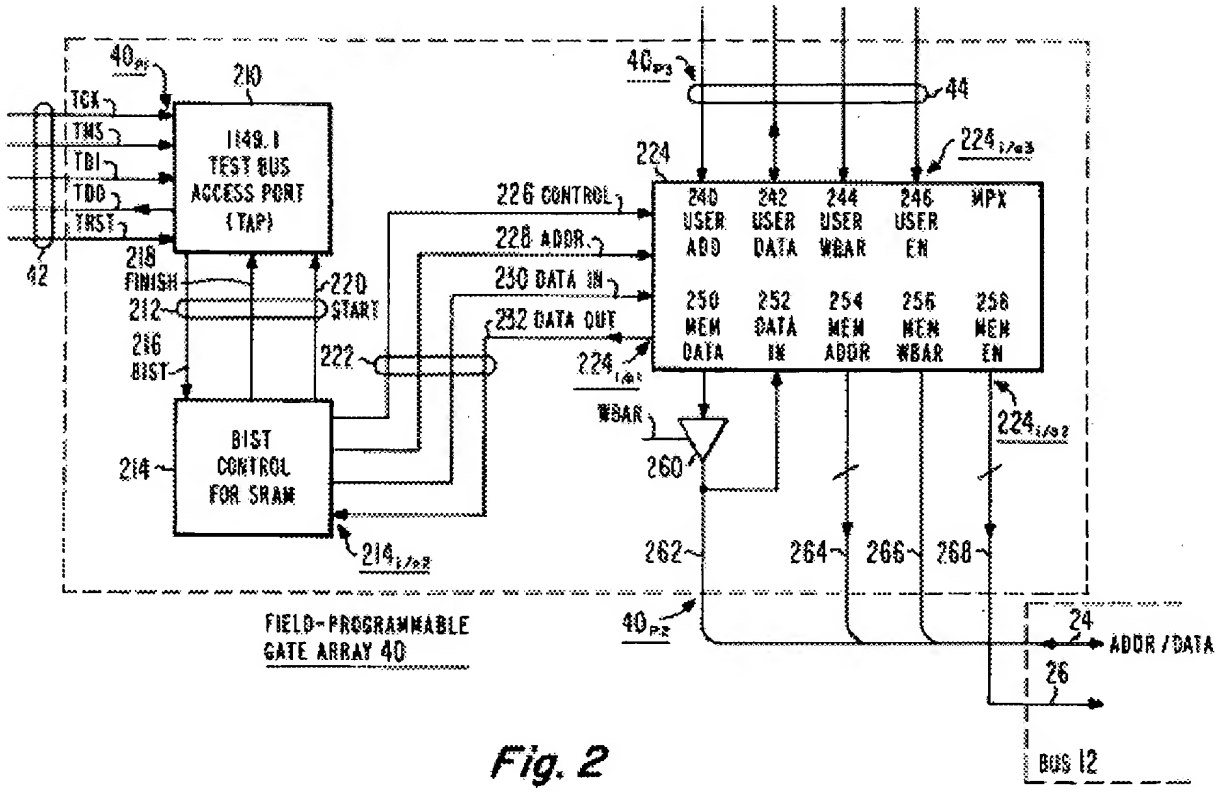


Fig. 2

operating mode. Thus, the FPGA is reconfigured into either (a) the configuration adapted to perform a particular function which is not a self-test or (b) a tester configuration for testing a

second type of logical function which is coupled to the communication bus. The assemblage, including the field-programmable gate array configured as one of (a) the configuration adapted to perform a particular function which is not a self-test and (b) a tester configuration for testing a second type of logical function which is coupled to the communication bus, is operated in one of (a) the normal mode and (b) ***in a manner which tests one of the second logical functions,*** *respectively. Thus, the assemblage can be operated in its normal operating mode, and then the FPGA can be reconfigured to test one device of one type, many devices of one type, or one device each of many types, or many devices of many types, following which normal operation can be resumed."... "Before beginning explanation of the operation of the arrangement of FIGS. 1 and 2, it should be noted that field programmable gate array 40 is essentially a "blank page"*

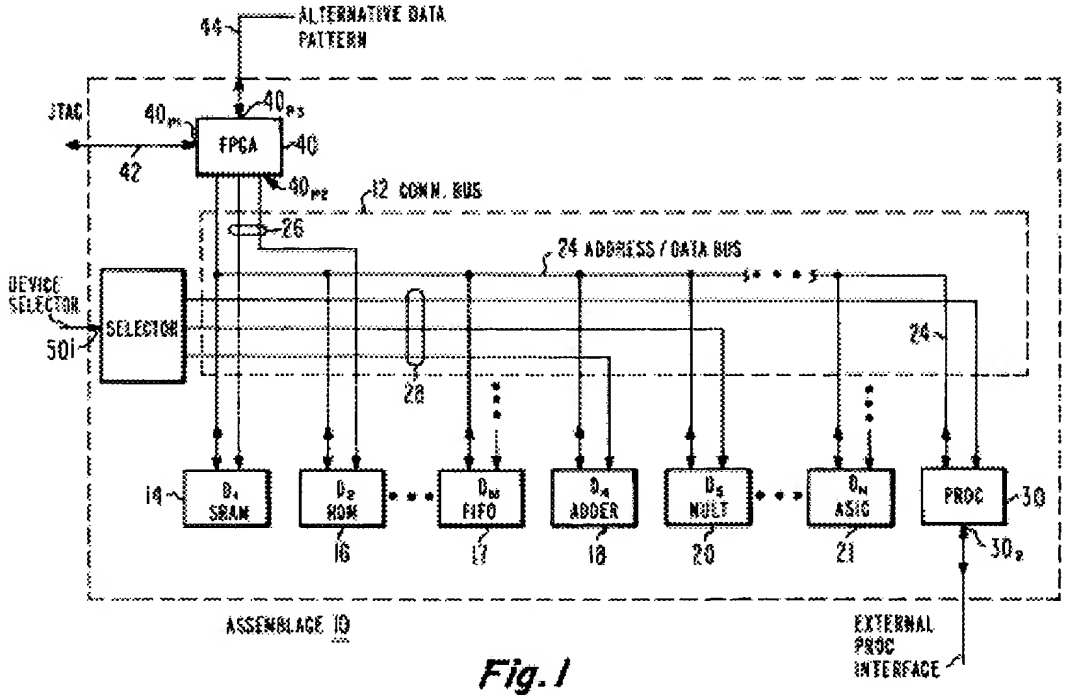


Fig. 1

in the absence of, or before, configuration. In the "blank page" state, the FPGA is no more than a grouping of unconnected gates or other basic electronic devices, with no discernible purpose. Thus, if the power to the assemblage 10 is interrupted, the configuration of FPGA 40 is lost, and it must be initially configured or "reconfigured" to the desired state before it can do anything. In the described embodiment,

the configuration information is applied by way of the test bus 42, which means that the configuration information required for the ordinary operating state of FPGA, ***for the memory self-test state, for the FIFO self-test state, and for the self-test states of the FPGA 40 as required for testing any known device 14-21,*** *where the hyphen represents the word "through," is stored in an outboard memory.* ***Those skilled in the art know that the configuration information could also be stored on-board the assemblage in some form of ROM, such as a UV-erasable ROM, or in nonvolatile RAM.*** *The described* ***embodiment, however, has the advantage that it requires no additional resources*** *(other than the outboard configuration information)* ***to perform self-test in addition to the function which it ordinarily performs.*** *Thus,* ***an assemblage such as that illustrated, with a field-programmable gate array, can be arranged to perform self-test without requiring significant additional resources on the assemblage itself,***" in col. 6 line 26 et seq.

As per Claims 1-20, Sharma et al. substantially discloses, in Figs. 1-3 and related description in col. 2 line 18 et seq., the claimed PLD or FPGA assembly comprising: programmable logic circuit or array in col. 2 line 42 and nonvolatile memory or store for testing in col. 2 line 26 with means to store configuration data in col. 2 line 49 in plural modes such as operation or test or modes in col. 2 line 49. JTAG access port is provided for test and data communication in col. 2 line 27 and means to integrate all PLD or FPGA assembly within on die or IC in col. 2 line 22. Means to reconfiguration circuit elements in col. 2 line 46 or col. 9 line 25 et seq., such in circuit elements seen e.g., in Fig. 1 as ROM or EEPROM mask read-only memory or ***UV-erasable ROM*** in col. 4 line 10-35 in a manner clear to those skilled in the art how to partition memory in plural sectors for storing data or self-test data. Means to start or boot up said assembly via commands or microprocessor control means in col. 4 line 31. **Sharma** 's Fig. 3 shows a procedure for FPGA assembly testing similar to the claimed invention of claims 11-20.

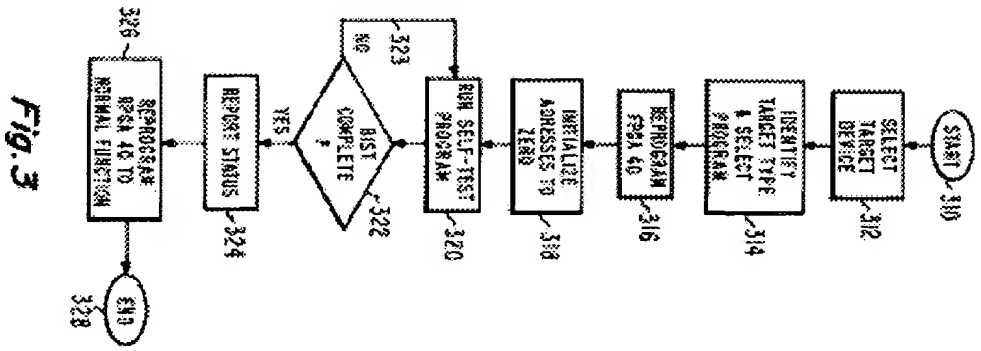
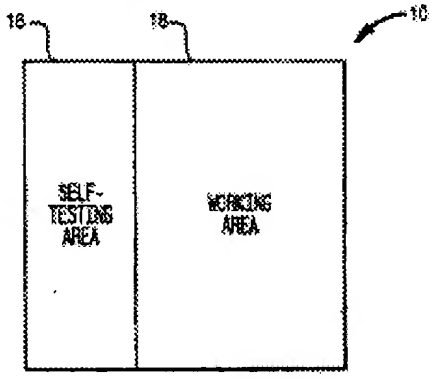


Fig. 3

Not specifically described in detail in **Sharma et al.** is the step of **self-testing within the** FPGA assembly. **However, Abramovici et al.** discloses such self-testing approach, e.g., in Figs. 2(below)-3 and col. 2 line 1 et seq.

Fig. 2



Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Sharma et al.** by including therein embedded **self-testing** as taught by **Abramovici et al.,** because such modification would provide the procedure disclosed in **Sharma et al.** with a technique wherein "*the need for external tester and human supervision associated therewith is obviated, thereby resulting in reduced testing cost.*" {See **Abramovici et al.,** col. 3 line 39 et seq.}

Conclusion

5. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for After-Final communications and for formal communications intended for entry),

(703) 746-5463 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.
Patent Examiner
3/6/04